

FIG. 1: prior art

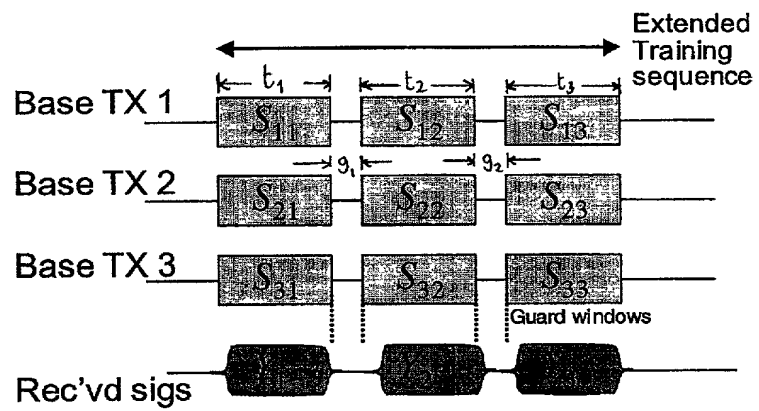
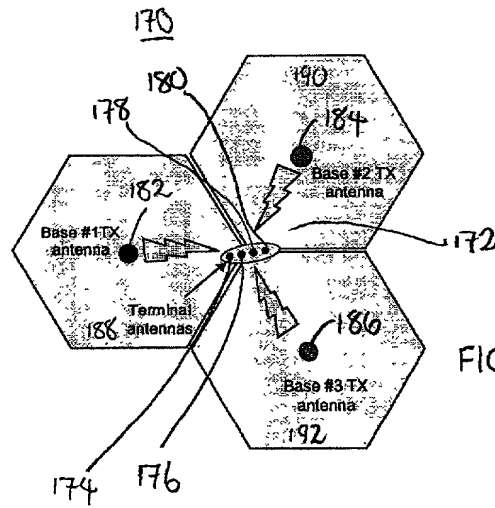
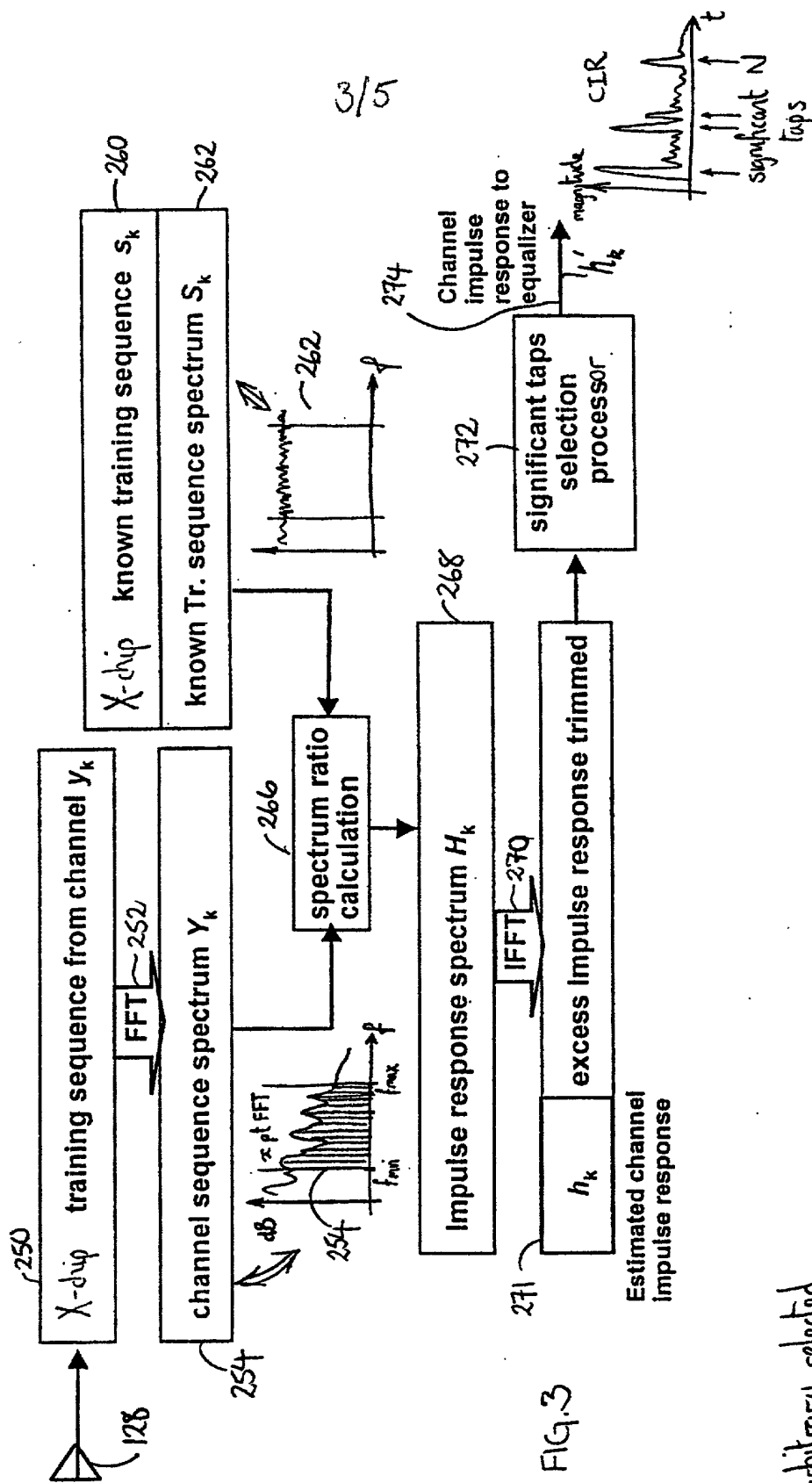


FIG. 4

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X=arbitrary selected number of chips in training sequence set by system standard.

500

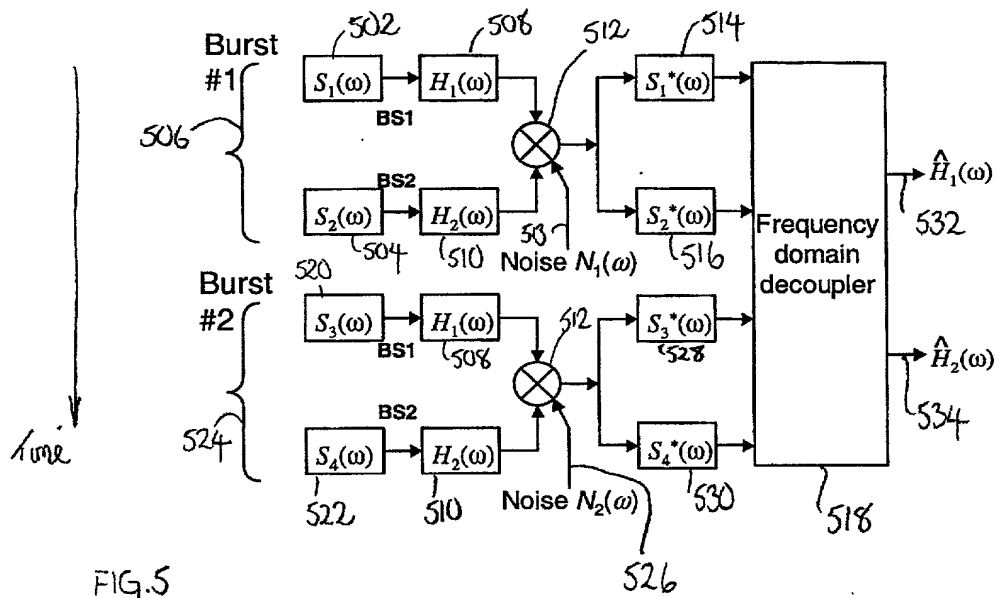


FIG. 5

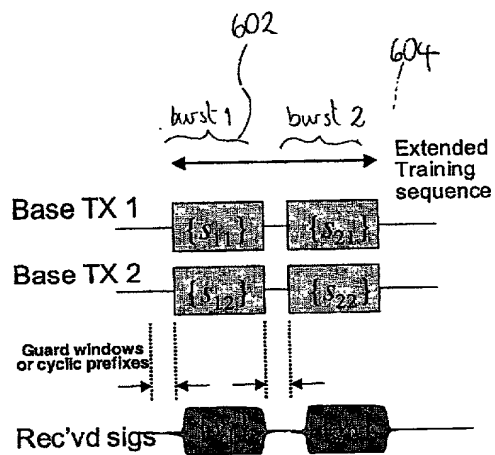


FIG. 6

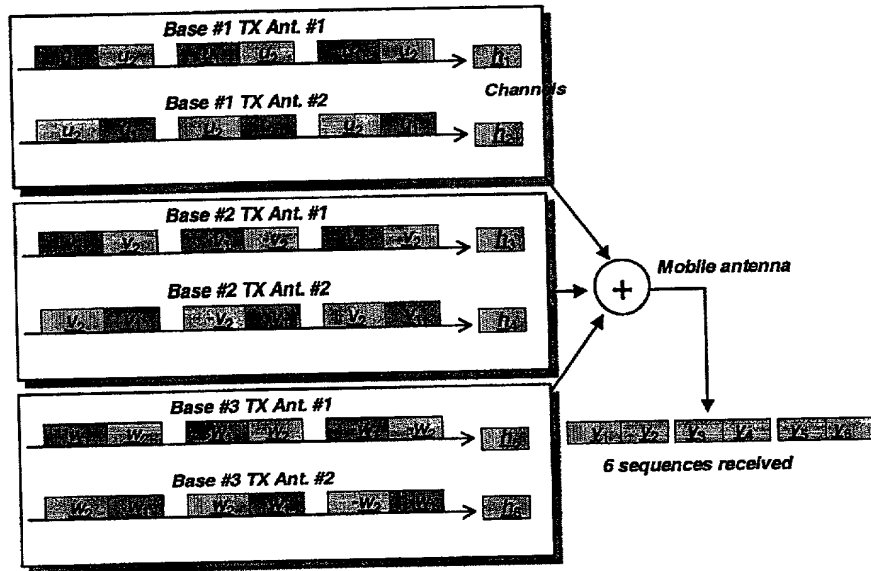


FIG. 7